

## Claims

What is claimed is:

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A1
- 1 1. A multibank DRAM macro, said macro comprising:
- 2 (a) a plurality of DRAM memory banks, each bank respectively
- 3 comprising:
- 4 (i) an array of DRAM memory cells,
- 5 (ii) bitlines and wordlines, respectively defining columns and
- 6 rows of the array,
- 7 (iii) a row address decoder circuit,
- 8 (iv) a column address decoder circuit,
- 9 (v) spare rows and columns for redundancy,
- 10 (b) a bank select input for each respective bank, each bank input
- 11 controlling operation of its respective bank, and
- 12 (c) a data path receiver / driver shared by at least two banks.
- 1 2. The DRAM macro of claim 1 further comprising (d) a master select input.
- 1 3. The DRAM macro of claim 2 wherein said bank select inputs are latched
- 2 to a falling edge of a signal from said master select input.
- 1 4. The DRAM macro of claim 1 wherein said macro further comprises a write
- 2 enable input.
- 1 5. The DRAM macro of claim 1 wherein said macro further comprises a page
- 2 mode select input.

- 1 6. The DRAM macro of claim 1 wherein each bank further comprises (vi) at  
2 least one sense amplifier.
- 1 7. The DRAM macro of claim 1 wherein each bank has capacity for about  
2 1 Mb of data.
- 1 8. The DRAM macro of claim 7 wherein said macro comprises at least 4 of  
2 said banks.
- 1 9. An integrated circuit device comprising a logic core and a DRAM macro  
2 wherein said DRAM macro is a multibank DRAM macro comprising:
- 3 (a) a plurality of DRAM memory banks, each bank respectively  
4 comprising:  
5 (i) an array of DRAM memory cells,  
6 (ii) bitlines and wordlines, respectively defining columns and  
7 rows of the array,  
8 (iii) a row address decoder circuit,  
9 (iv) a column address decoder circuit ,  
10 (v) spare rows and columns for redundancy,
- 11 (b) a bank select input for each respective bank, each bank input  
12 controlling operation of its respective bank, and
- 13 (c) a data path receiver / driver shared by at least two banks.

1 10. The integrated circuit device of claim 9 wherein said DRAM macro further  
2 comprises (d) a master select input.

1 11. The integrated circuit device of claim 10 wherein said bank select inputs  
2 are latched to a falling edge of a signal from said master select input.

1 12. The integrated circuit device of claim 9 wherein said DRAM macro further  
2 comprises a write enable input.

1 13. The integrated circuit device of claim 9 wherein said DRAM macro further  
2 comprises a page mode select input.

1 14. The integrated circuit device of claim 9 wherein each bank of said DRAM  
2 macro further comprises (vi) at least one sense amplifier.

1 15. The integrated circuit device of claim 9 wherein each bank of said DRAM  
2 macro has capacity for about 1 Mb of data.

1 16. The integrated circuit device of claim 15 wherein said DRAM macro  
2 comprises at least 4 of said banks.